TSMC-01-1674

February 9, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/706,380 11/12/03

Cliff Hou et al.

A METHODOLOGY TO OPTIMIZE HIER-ARCHICAL CLOCK SKEW BY CLOCK DELAY COMPENSATION

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February , 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B Ackerman 2/12/04

"Clock Generation and Distribution for the First IA-64 Microprocessor," Tam et al., IEEE Journal of Solid-State Circuits, pp. 1545-1552, Nov. 2000, Vol. 35, No. 11, ISSN: 0018-9200, describes clock distribution with an active distributed deskewing technique.

"Performance Optimization of VLSI Interconnect Layout," Cong et al., The Journal of VLSI Integration, Vol. 21, Nos. 1&2, Nov. 1996, pp. 1-99, presents a comprehensive survey of existing techniques for interconnect optimization during the VLSI physical design process.

"An Algorithm for Zero-Skew Clock Tree Routing with Buffer Insertion," Chen et al., Proceeding - European Design and Test Conf., pp. 1-22, 1996, presents multi-stage zero skew clock tree construction for minimizing clock phase delay and wire-length.

"Physical Design CAD in Deep Sub-micron Era," Mitsuhashi et al., Proceedings of the European Design Automation Conf. with EURO-VHDL'96, Geneva, Switzerland, IEEE Computer Society Press, Los Alamitos, CA, pp. 350-355, ISBN:0-8186-7573-X, describes timing optimization and power minimization methods using the concept are discussed in detail.

"Wire Segmenting for Improved Buffer Insertion," Alper et al., Proceedings of the 34th Annual ACM/IEEE Design Automation Conf., 1997, ACM Press, New York, NY, USA, pp. 588-593 ISBN: 0-89791-920-3, presents buffer insertion, which seeks to place buffers on the wires of a signal net to minimize delay.

"Repeater Block Planning under Simultaneous Delay and Transition Time Constraints," Sarkar et al., Proceedings 2001 European Design, Automation and Test Conf., March 2001, pp. 540-544, describes a solution to the problem of repeater block planning under both delay and signal transition time constraints for a given floor plan.

U.S. Patent 6,311,314 to McBride, "System and Method for Evaluating the Loading of a Clock Driver," describes a system and method for evaluating the loading of a clock driver.

U.S. Patent 6,053,950 to Shinagawa, "Layout Method for a Clock Tree in a Semiconductor Device," teaches a layout method for a clock tree in a clock signal distribution circuit.

U.S. Patent 6,020,774 to Chiu et al., "Gated Clock Tree Synthesis Method for the Logic Design," demonstrates a gated clock tree synthesis (CTS) method for the purpose of synthesizing a gate array logic circuit to allow optimal topological arrangement of the gate array on the logic circuit.

U.S. Patent 5,864,487 to Merryman et al., "Method and Apparatus for Identifying Gated Clocks within a Circuit Design Using a Standard Optimization Tool," illustrates a method and apparatus for identifying gated clocks within a circuit design using a standard optimization tool.

U.S. Patent 5,686,845 to Erdal et al., "Hierarchial Clock Distribution System and Method," describes a hierarchical clock distribution system and method.

U.S. Patent 6,473,890 to Yasui et al., "Clock Circuit and Method of Designing the Same," discloses a clock circuit utilizing a clock delay and a method of designing the same.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-01-1674	10/706,380
Applicant: Cliff Hou et al.	
Filing Date: 11/12/03	Group Art Unit

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6,311,314	10/30/01	McBride	716	6	4/27/99
	6,053,950	4/25/00	Shinagawa	716	2	2/13/98
	6,020,774	2/1/00	Chiu et al.	327	295	7/23/98
	5,864,487	1/26/99	Merryman et al.	364	491	11/19/96
	5,686,845	11/11/97	Erdal et al.	326	93	8/28/96
	6,473,890	10/29/02	Yasui et al.	716	10	9/18/00

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- "Clock Generation and Distribution for the First IA-64 Microprocessor," Tam et al. IEEE Jrnl of Solid-State Circuits, pp. 1545-1552, Nov. 2000, Vol. 35, No. 11, ISSN: 0018-9200.
- "Performance Optimization of VLSI Interconnect Layout", Cong et al., The Jrnl of VLSI Integration, Vol. 21, Nos. 1-2, Nov. 1996, pp. 1-99.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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– "An Algorithm for Zero-Skew Clock Tree Routing with Buffer Insertion", Chen et al., Proceeding-European Design and Test Conf., pp. 1-22, 1996.

– "Physical Design CAD in Deep Sub-micron Era", Mitsuhashi et al., Proceedings of the European Design Automation Conf. w/EURO-VHDL'96, Geneva, Switzerland, IEEE Comp. Soc. Press, CA, pp. 350-355, ISBN: 0-8186-7573-X.

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